

# PA15FL • PA15FLA

## FEATURES

- HIGH VOLTAGE — 450V ( $\pm 225V$ )
- LOW COST
- LOW QUIESCENT CURRENT — 3.0mA MAX
- HIGH OUTPUT CURRENT — 200mA
- PROGRAMMABLE CURRENT LIMIT

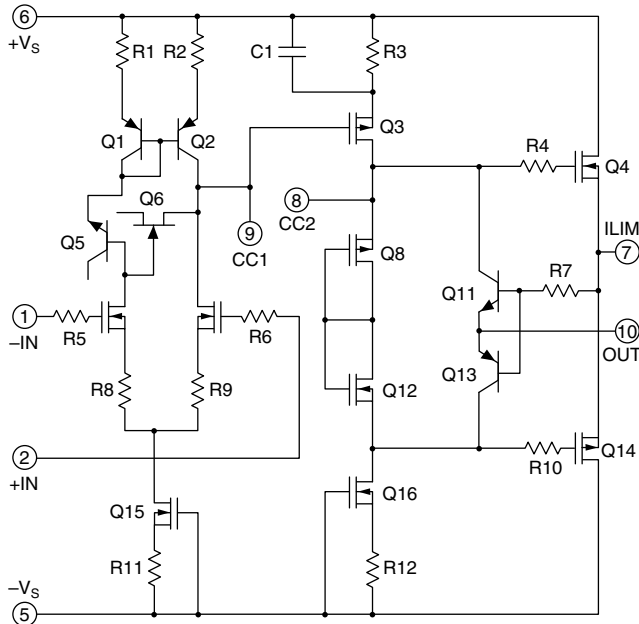
## APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V

## DESCRIPTION

The PA15FL is a high voltage, low quiescent current MOSFET operational amplifier designed as a low cost solution for driving continuous output currents up to 200mA and pulse currents up to 350mA into capacitive loads. The safe operating area (SOA) has no second breakdown limitations and can be observed for all type loads by choosing an appropriate current limiting resistor. The MOSFET input stage has integrated static and differential mode protection. The MOSFET output stage is biased AB for linear operation. External compensation provides flexibility in choosing bandwidth and slew rate for the application. The 10-pin power SIP package is electrically isolated.

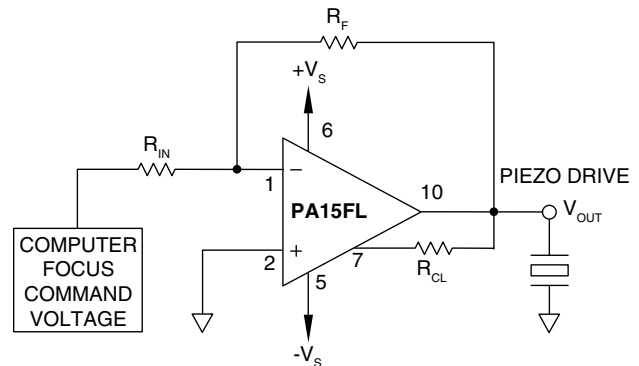
## EQUIVALENT SCHEMATIC



## 10-PIN SIP PACKAGE STYLE FL

Formed leads available  
See package style FU

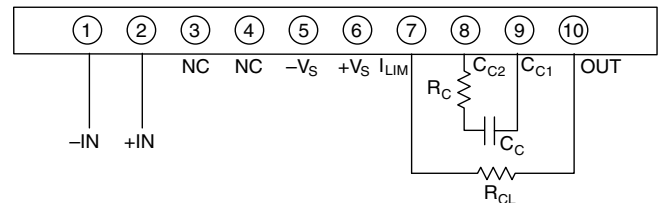
## TYPICAL APPLICATION



## LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA15FL reduces the costs of power supplies and cooling with its advantages of low cost and low quiescent power consumption while increasing circuit density with the SIP package.

## EXTERNAL CONNECTIONS



## PHASE COMPENSATION

GAIN	$C_C$	$R_C$
$\geq 1$	33pf	1K $\Omega$
$\geq 10$	OPEN	OPEN

$$R_{CL} \cong \frac{.6}{I_{CL}}$$

# PA15FL • PA15FLA

ABSOLUTE MAXIMUM RATINGS  
SPECIFICATIONS

## ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ $T_C = 25^\circ\text{C}$	30W
INPUT VOLTAGE, differential	$\pm 25\text{V}$
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	$260^\circ\text{C}$
TEMPERATURE, junction <sup>2</sup>	$150^\circ\text{C}$
TEMPERATURE RANGE, storage	$-40$ to $+85^\circ\text{C}$
OPERATING TEMPERATURE RANGE, case	$-25$ to $+85^\circ\text{C}$

## SPECIFICATIONS

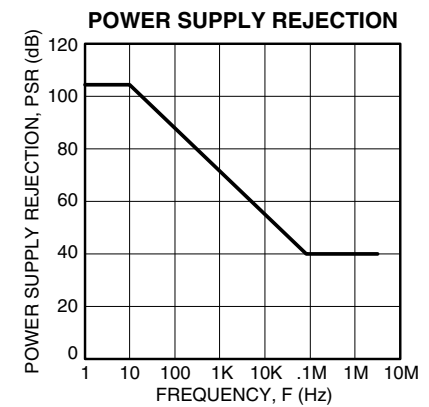
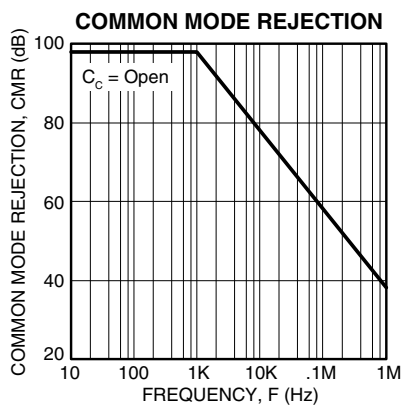
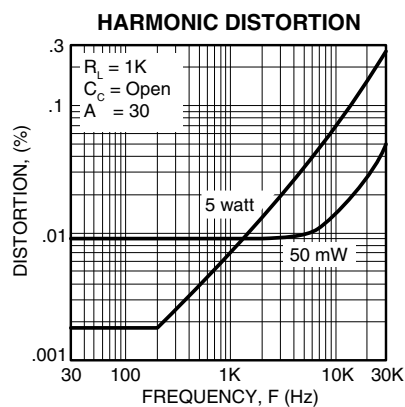
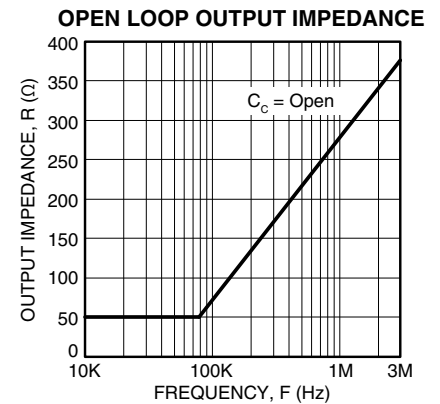
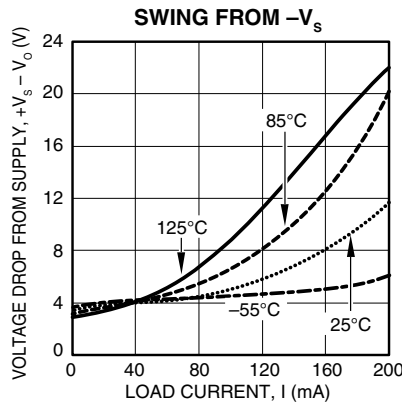
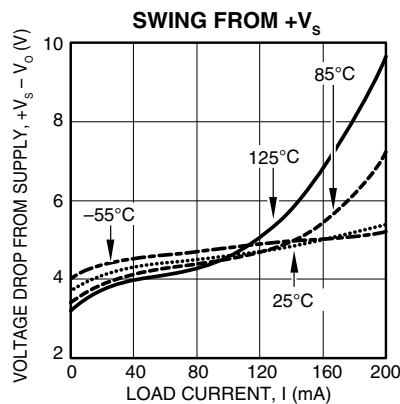
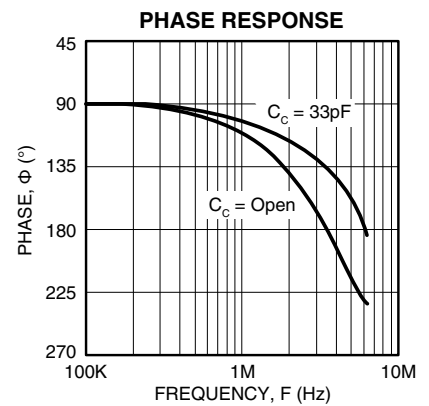
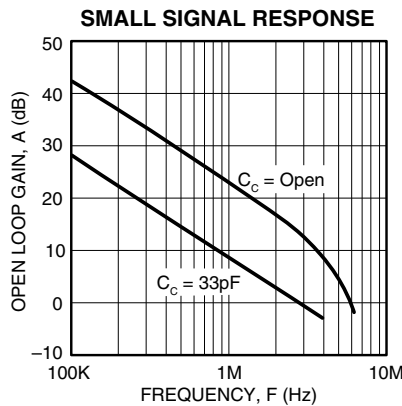
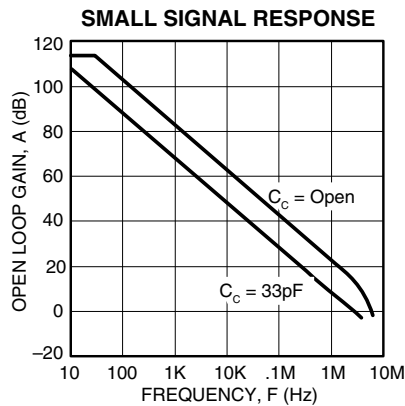
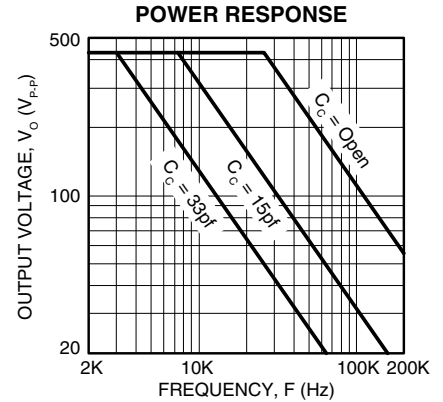
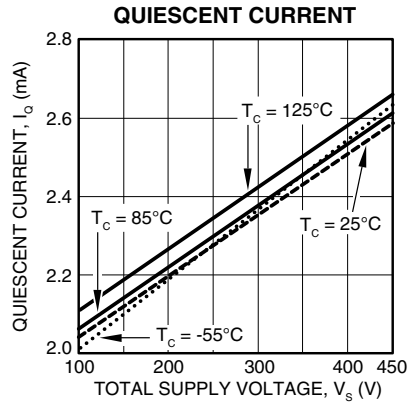
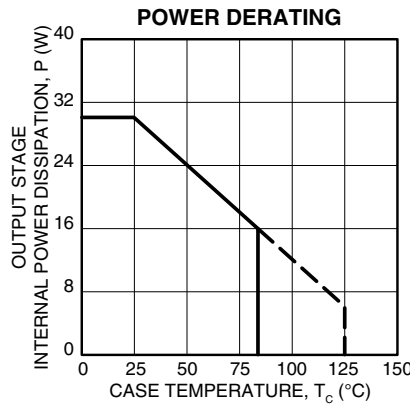
PARAMETER	TEST CONDITIONS <sup>1</sup>	PA15FL			PA15FLA			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>INPUT</b>									
OFFSET VOLTAGE, initial	Full temperature range		2	10		.5	3	mV	
OFFSET VOLTAGE, vs. temperature			15	50		5	20	$\mu\text{V}/^\circ\text{C}$	
OFFSET VOLTAGE, vs. supply				10	50		*	*	$\mu\text{V}/\text{V}$
OFFSET VOLTAGE, vs. time				75			*	*	$\mu\text{V}/\sqrt{\text{kh}}$
BIAS CURRENT, initial				200	2000		*	*	pA
BIAS CURRENT, vs. supply				4			*	*	pA/V
OFFSET CURRENT, initial			50	500		30	200	pA	
INPUT IMPEDANCE, DC			$10^{11}$			*		$\Omega$	
INPUT CAPACITANCE			4			*		pF	
COMMON MODE VOLTAGE RANGE <sup>3</sup>	$V_{CM} = \pm 90\text{V}$ 10KHz BW, $R_S = 1\text{K}\Omega$ , $C_C = \text{OPEN}$	$\pm V_S - 15$			*			V	
COMMON MODE REJECTION, DC		80	98		*	*		dB	
NOISE			2			*		$\mu\text{V}_{\text{rms}}$	
<b>GAIN</b>									
OPEN LOOP, @ 15Hz	$R_L = 2\text{K}\Omega$ , $C_C = \text{OPEN}$ $R_L = 2\text{K}\Omega$ , $C_C = \text{OPEN}$ $R_L = 2\text{K}\Omega$ , $C_C = \text{OPEN}$ Full temperature range	94	111		*	*		dB	
GAIN BANDWIDTH PRODUCT at 1MHz				5.8		*	*	MHz	
POWER BANDWIDTH				24		*	*	kHz	
PHASE MARGIN				60		*	*	$^\circ$	
<b>OUTPUT</b>									
VOLTAGE SWING <sup>3</sup>	$I_O = \pm 200\text{mA}$ $C_C = \text{OPEN}$ Full temperature range $C_C = \text{OPEN}$ , 2V step	$\pm V_S - 15$	$\pm V_S - 10$		*	*		V	
CURRENT, continuous		$\pm 200$			*			mA	
SLEW RATE, $A_V = 100$			20		20	30		V/ $\mu\text{s}$	
CAPACITIVE LOAD, $A_V = +1$			100		*			pf	
SETTLING TIME to .1%				2		*		$\mu\text{s}$	
RESISTANCE, no load				50		*		$\Omega$	
<b>POWER SUPPLY</b>									
VOLTAGE <sup>5</sup>	See note 5	$\pm 50$	$\pm 150$	$\pm 225$	*	*	*	V	
CURRENT, quiescent,				2.0	3.0		*	*	mA
<b>THERMAL</b>									
RESISTANCE, AC, junction to case <sup>4</sup>	Full temperature range, $F > 60\text{Hz}$ Full temperature range, $F < 60\text{Hz}$ Full temperature range Meets full range specifications			2.5			*	$^\circ\text{C}/\text{W}$	
RESISTANCE, DC, junction to case					4.2			*	$^\circ\text{C}/\text{W}$
RESISTANCE, junction to air				30			*	*	$^\circ\text{C}/\text{W}$
TEMPERATURE RANGE, Case			$-25$		$+85$	*		*	$^\circ\text{C}$

- NOTES: \* The specification of PA15FLA is identical to the specification for PA15FL in applicable column to the left.
- Unless otherwise noted:  $T_C = 25^\circ\text{C}$ , compensation =  $C_C = 33\text{pF}$ ,  $R_C = 1\text{K}\Omega$ ,  $R_{CL} = 0$ . DC input specifications are  $\pm$  value given. Power supply voltage is typical rating.
  - Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
  - $+V_S$  and  $-V_S$  denote the positive and negative power supply rail respectively.
  - Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
  - Derate max supply rating .625 V/ $^\circ\text{C}$  below  $25^\circ\text{C}$  case. No derating needed above  $25^\circ\text{C}$  case.

### CAUTION

The PA15FL is constructed from MOSFET transistors. ESD handling procedures must be observed.

The exposed substrate contains beryllia (BeO). Do not crush, machine, or subject to temperatures in excess of  $850^\circ\text{C}$  to avoid generating toxic fumes.



### GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit [www.apexmicrotech.com](http://www.apexmicrotech.com) for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit; heat sink selection; Apex's complete Application Notes library; Technical Seminar Workbook; and Evaluation Kits.

### CURRENT LIMIT

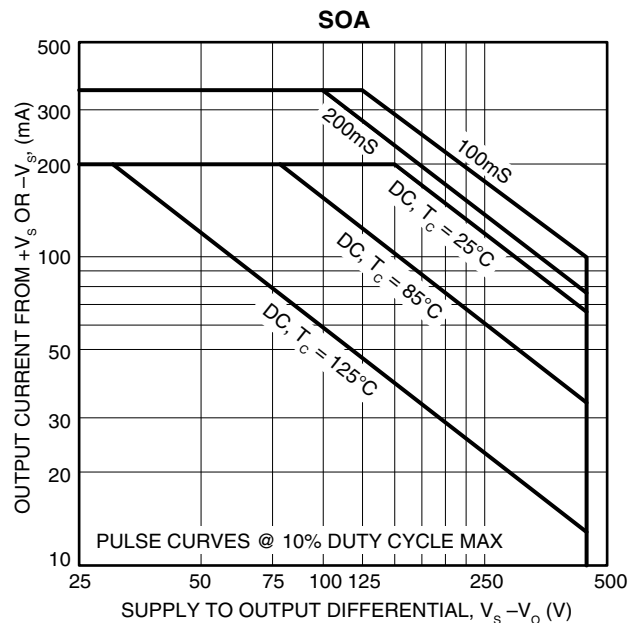
For proper operation, the current limit resistor ( $R_{CL}$ ) must be connected as shown in the external connection diagram. The minimum value is 2 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.6}{I_{LIM}}$$

### SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



### INPUT PROTECTION

Although the PA15FL can withstand differential input voltages up to  $\pm 25\text{V}$ , additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1-D4 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1-Q4 in Figure 2b). In either case the input differential volt-

age will be clamped to  $\pm 1.4\text{V}$ . This is sufficient overdrive to produce maximum power bandwidth.

### POWER SUPPLY PROTECTION

Unidirectional zener diode transient suppressors are recommended as protection on the supply pins. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation.

Conditions which can cause open circuits or polarity reversals on either power supply rail should be avoided or protected against. Reversals or opens on the negative supply rail are known to induce input stage failure. Unidirectional transzors prevent this, and it is desirable that they be both electrically and physically as close to the amplifier as possible.

### STABILITY

The PA15FL has sufficient phase margin to be stable with most capacitive loads at a gain of 10 or more, using the recommended phase compensation.

The PA15FL is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor  $C_c$  must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network  $C_c R_c$  must be mounted closely to the amplifier pins 8 and 9 to avoid spurious oscillation.

FIGURE 2. OVERVOLTAGE PROTECTION

